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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,476	02/02/2001	Esin Terzioglu	37115/JFO/B600	7751

7590

09/16/2002

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EXAMINER

PHAN, TRONG Q

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 09/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.  
**09/775,476**

Applicant(s)  
**TERZIOGLU ET AL.**

Examiner  
**TRONG PHAN**

Art Unit  
**2818**



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Aug 19, 2002
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above, claim(s) 3, 5, 11 and 17 have been canceled is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4, 6-10, and 12-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on Aug 19, 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some\* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_ 6) ☐ Other:

***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 6-10 and 12-16 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The invention as recited in claims 6-10 and 12-16 are not understood because of the following reasons:

- a) elements 608a-b and 640 in Fig. 6 are not described in the specification;
- b) elements M1-M7, M10-M12, M16 and I13 in fig. 8 are not described in the specification;
- c) Fig. 11 of the present invention is not described;
- d) elements PREDECODER and GWD in Fig. 12 are not described in the specification;
- e) elements shift, shutOutH, shift\_n\_Prev, xL\_Prev, x1, x2\_n, x2\_n\_Prev, PREV CKT, shutinH, shift\_n and 1703 in Fig. 17 are not described in the specification;
- f) elements del,1:6>, Ineg<0:2>, RO\_div64, lpos<0:2>, 1955 and 1958 in Fig. 19 are not described in the specification;
- g) elements DRD, 2125, 2135 and 2137 in Fig. 21 are not described in the specification;

h) elements MN11, MN21, 2264 and 2274 in Fig. 22B are not described in the specification;

i) it is not understood how the redundancy selector circuit in Figs. 16-17 can be a column redundancy selector circuit which can be incorporated with the memory structure in Fig. 12 and as described in lines 6-9, page 9 of Amendment A and in lines 31-34, page 39 of the specification. Since all the row lines of the memory structure in Fig. 12 are shown to be connected to only GWD and LWD circuits and all the column lines of the memory structure in Fig. 12 are shown to be connected to only LSA circuit.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 6, 9 and 12-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6, it is not clear what element in the first and second memory cell groups the decoder decodes (paragraph d).

Claim 9, it is not clear how the group-select signal can be an alternative-column-select signal (last two lines) since Figs. 16 and 17 of the present invention show that the circuit providing the claimed group-select signal is associated with the word line WL only.

Claim 12, it is not clear what element in the first and second memory cell groups the decoder decodes (paragraph g).

Claim 13, it is not clear what element in the first and second memory cell

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groups the decoder decodes.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2 and 4 are, insofar as understood, rejected under 35 U.S.C. 102(b) as being anticipated by Tomita, 5,886,941.

Tomita, 5,886,941, discloses in Fig. 1 an address decoder for a memory device comprising:

an asynchronous portion comprising decoding circuits i0-i255 coupled with word lines W0-W255;

a synchronous portion coupled to receive and respond to clock signal CK,

a feedback-resetting portion comprising control circuit 1 which, as shown in Fig. 4, includes an asynchronous reset signal R from the output of NAND gate 105.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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8. Claims 6-10 and 12-16 are, insofar as understood, rejected under 35 U.S.C. 103(a) as being unpatentable over Akizawa et al., 5,398,206, in view of Tomita, 5,886,941.

Akizawa et al., 5,398,206, discloses in Fig. 16 a memory module (see lines 16-19, column 13) comprising:  
address decoder 100;  
word line selection detecting circuit 200 being control by group select signals 205 and 206;  
first memory cell group 310;  
second memory cell group 320.

What is not shown in Fig. 16 of Akizawa et al., 5,398,206, is the address decoder as recited in claim 12.

Tomita, 5,886,941, discloses in Fig. 1 an address decoder for a memory device comprising:  
an asynchronous portion comprising decoding circuits i0-i255 coupled with word lines W0-W255;  
a synchronous portion coupled to receive and respond to clock signal CK,  
a feedback-resetting portion comprising control circuit 1 which, as shown in Fig. 4, includes an asynchronous reset signal R from the output of NAND gate 105.

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the address decoder in Figs 1 and 4 of Tomita, 5,886,941, for the address decoder 100 in Fig. 16 of Akizawa et al.,

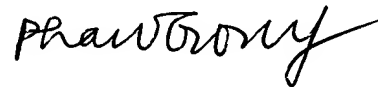
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5,398,206, for the purpose of high speed operation without malfunction (see lines 1-6, column 4 of Tomita, 5,886,941).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (703) 308-4870. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-4021 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



**TRONG PHAN  
PRIMARY EXAMINER**

September 10, 2002